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EXAMINER	
RIYAMI, ABDULLA A	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/767,234	GULSTONE, NIGEL A.	
	Examiner	Art Unit	
	ABDULLAH RIYAMI	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *28 January 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Autechaud et al. (6321361) in view of Turner (7305047).

As per claim 1, Autechaud et al. discloses a method of processing data of a data communication channel (see abstract and figure 1), comprising: de-multiplexing serial data from each of the serial data signals received from the lanes and formatting the data of the lanes into parallel data (see figure 1, decoder 108r, deserializer 109r, column 6-8); checking the parallel data for a start-of-frame (SOF) character (see figure 1, 1021r column 2, 6, 8); responsive to the checking for a SOF character, parsing the parallel data into non-data and real data (see column 10, idle or null character is detected, real data SOF and EOF is checked); basing the parsing of the parallel data at least in part on placement relative to the SOF character (see column 10); packing the parsed real data into a group of data (see column 10); presenting the packed group of data; and activating a start-of-frame sideband signal when beginning the presenting the packed group data (see column 2 and figure 1, 1021r-101r).

Autechaud does not expressly disclose receiving a plurality of serial data signals from lanes of the communication channel.

Turner discloses receiving a plurality of serial data signals from lanes of the communication channel (see figure 11 and 20, column 2, 4).

Autechaud and Turner are analogous art since they are from the same field of endeavor of detecting and checking SOF and EOF in receivers.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to use Turner's lane assignment technique in Autechaud's device for checking and detecting SOF and EOF in receivers. The motivation being having a fair utilization of the method and apparatus of the high speed communication receiver by using a plurality of de-serializers, along with detecting and checking SOF and EOF in the receiver.

As per claim 2, Autechaud et al. discloses a method of processing data of a data communication channel (see abstract and figure 1), further comprising: checking the parallel data for an end-of-frame (EOF) character; the parsing the parallel data to comprise determining if a character of the parallel data is outside a frame bounded by the SOF and the EOF characters, and if the character is determined outside the frame, defining the character as non-data (see column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 3, Autechaud et al. discloses a method of processing data of a data communication channel (see abstract and figure 1), the parsing further to define the SOF and EOF characters as non-data (see column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 4, Autechaud et al. discloses a method of processing data of a data communication channel (see abstract and figure 1), the parsing further to comprise: checking for idle characters between the SOF and the EOF characters, and responsive to the checking for idle characters, defining the idle characters as non-data (see column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 5, Autechaud et al. discloses a method of processing data of a data communication channel (see abstract and figure 1), in which the packing configures the real data into a contiguous group (see column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 6, Autechaud et al. discloses a method of processing data of a data communication channel (see abstract and figure 1), further comprising activating an end-of-

frame sideband signal when sending out a last portion of the contiguous group (see figure 1 1021r-101r).

As per claim 7, Autechaud et al. discloses a method of processing data of a data communication channel (see abstract and figure 1), in which the packing comprises aligning the real data of the contiguous group with one of a left or a right alignment relative to at least one of the SOF and EOF sideband signals (see column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 8, Autechaud et al. discloses a method of processing data of a data communication channel (see abstract and figure 1), in which the receiving comprises receiving sequential words each having a byte width proportional to the number of lanes; the checking for the EOF character comprises examining bytes in a first word including the SOF character; and if the EOF character is not found, the method further comprising repeating for subsequent words the receiving, de-multiplexing, parsing and packing until finding an EOF character (see column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 9, Autechaud et al. discloses a method of processing data of a data communication channel (see abstract and figure 1), in which the received sequential words comprise characters of left to right relationship corresponding to time-ordered placement of the characters (see column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 10, Autechaud et al. discloses a method of processing data of a data communication channel (see abstract and figure 1), further comprising performing at least one of storing and outputting data based on the number of characters previously packed, the amount of

new real data packed during the repeating, and the size of the output (see column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 11, Autechaud et al. discloses a method of processing data of a data communication channel (see abstract and figure 1), in which the new real data is stored when the total real data is less than or equal the size of the output, and when the EOF character has not been found (see figure 1, receiving buffer).

As per claim 12, Autechaud et al. discloses a method of processing data of a data communication channel (see abstract and figure 1), in which a portion of the new real ~ data is output together with previously packed data, and a remaining portion of the new real data is stored when the total real data exceeds the size of the output (see column 10, idle or null character is detected, real data SOF and EOF is checked (regular buffering technique)).

As per claim 13, Autechaud et al. discloses a method in which the packed data is output when an EOF character has been found (see column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 14,Turner discloses a method in which identifying a number of lanes in the communication channel; and configuring serial-to-parallel data receivers to receive and de-multiplex the serial data signals of the identified lanes to form output characters for the parallel data (see figure 11 and 20, column 2, 4).

As per claim 15, Autechaud et al. discloses a circuit to interface a communications channel (see abstract and figure 1) comprising:

a decoder to determine character types of the characters recovered by the receivers of the data lanes (see figure 1, decoder 108r, deserializer 109r, column 6-8);

detectors to detect at least one of a start-of-frame (SOF) character and an end-of-frame (EOF) character see figure 1, 1021r, column 2, 6 and 8);

parser to parse characters recovered by the receivers based on the character types determined by the decoders and placement relative to a detected SOF character; and a packer to group the parsed characters (see column 10, idle or null character is detected, real data SOF and EOF is checked).

Autechaud does not expressly disclose a plurality of serial-to-parallel receivers to receive serial data signals of data lanes of the communications channel and recover characters of parallel format from the data lanes and a plurality of decoders.

Turner discloses a plurality of serial-to-parallel receivers to receive serial data signals of data lanes of the communications channel and recover characters of parallel format from the data lanes and a plurality of decoders (see figure 11 and 20, column 2, 4).

Autechaud and Turner are analogous art since they are from the same field of endeavor of detecting and checking SOF and EOF in receivers.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to use Turner's lane assignment technique in Autechaud's device for checking and detecting SOF and EOF in receivers. The motivation being having a fair utilization of the method and apparatus of the high speed communication receiver by using a plurality of de-serializers, along with detecting and checking SOF and EOF in the receiver.

As per claim 16, Autechaud et al. discloses a circuit (see abstract and figure 1), in which the decoders resolve character types of the group consisting of at least one of SOF, EOF, real data and idle data characters; and the parser to invalidate characters determined to be outside a

frame delineated by at least one of a detected SOF character and a detected EOF character (see column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 17, Autechaud et al. discloses a circuit (see abstract and figure 1), in which the packer comprises aligning the real data of the contiguous group with one of a left or a right alignment (see column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 18, Autechaud et al. discloses a circuit (see abstract and figure 1), the parser and the packer further to group the packed data characters into a contiguous block, the contiguous block having no idle characters between real data characters.

As per claim 19, Autechaud et al. discloses a circuit (see abstract and figure 1), further comprising: storage registers accessible to store characters for subsequent retrieval; and a storage controller to transfer the aligned data characters to the storage registers if the detectors determine absence of an EOF character (see figure 1, column 2, 5-8, column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 20, Autechaud et al. discloses a circuit (see abstract and figure 1), further comprising: a data output port having a word width; and in which the storage controller is further operable to determine a first amount of the aligned data characters, a second amount of data characters retained in the storage registers, and if a total of the first and second amounts is greater than the word width of the output port, to transfer at least a portion of the aligned data characters to the storage registers (see figure 1, column 2, 5-8, column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 21, Autechaud et al. discloses a circuit (see abstract and figure 1), further comprising an output controller to enable transfer of data characters to the output port responsive

to at least one of the detector detecting an EOF character and the storage controller determining that the total is at least equal to the word width of the output port (see figure 1 1021r-101r).

As per claim 22, Autechaud et al. discloses a circuit (see abstract and figure 1), in which the storage controller and output controller are further operable, responsive to determining the total is greater than the word width of the output port, to take characters from the storage registers and a portion of the aligned data characters to form and present an output word on the output port (see figure 1, column 2, 5-8, column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 23, Autechaud et al. discloses a circuit (see abstract and figure 1),, in which the storage controller and output controller are further operable to write a remaining portion of the aligned real characters into the storage registers (see figure 1, column 2, 5-8, column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 24, Turner discloses a system to interface a communication channel having a plurality of serial data lanes (abstract and figures 11 and 20), comprising:

a plurality of receivers to receive the serial data from the~ data lanes, each receiver comprising a serial-to-parallel converter to convert received serial data to parallel format (see figures 11 and 20);

the plurality of receivers comprising outputs that collectively form a word having a width related to the number of data lanes (see figures 12-19 column 2,lines 46-67 and columns 4-6);

decoders to identify character types recovered by the receivers (see figures 11, 20, column 2,lines 46-67); logic to determine when a decoder of the decoders has identified at least one of the character types of the group consisting of a start-of-frame and an end-of-frame character;

parsing circuitry to determine valid characters of the word based upon placement relative to the identified start-of- frame character and the end-of-frame character (column 2 and 4-6), a storage register selectively operable to receive characters that have been determined valid by the parser (see column 4-6, figure 27, 20 and 21) .

Turner does not expressly disclose a controller to control presentment of determined valid data to at least one of the storage registers or an output port, the presentment based on character types identified by the decoders, the placements relative the SOF character, a first amount of the valid characters determined by the parsing circuitry, and a second amount of characters stored in the storage registers.

Autechaud discloses a controller to control presentment of determined valid data (see figure 1, block 101r) to at least one of the storage registers or an output port, the presentment based on character types identified by the decoders , the placements relative the SOF character, a first amount of the valid characters determined by the parsing circuitry, and a second amount of characters stored in the storage registers (see figure 1, column 2, 5-8, column 10, idle or null character is detected, real data SOF and EOF is checked).

Turner and Autechaud are analogous art since they are from the same field of endeavor of detecting and checking SOF and EOF in receivers.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to use Turner's lane assignment technique in Autechaud's device for checking and detecting SOF and EOF in receivers. The motivation being having a fair utilization of the method and apparatus of the high speed communication receiver by using a plurality of de-serializers, along with detecting and checking SOF and EOF in the receiver.

As per claim 25, Autechaud et al. discloses a system, further comprising a generator to present a sideband start-of-frame signal to accompany valid data at the output port when first presented (see column 2 and figure 1, 1021r-101r).

As per claim 26, Autechaud discloses the generator further to present a sideband end-of-frame signal to accompany parsed valid data at the output port when the decoder and the logic have determined an EOF character and the controller enabled presentment of valid data of a word associated with the EOF character (see column 2 and figure 1, 1021r-101r).

As per claim 27, Autechaud discloses the generator to further present a data valid signal when parsed valid data and the accompanying EOF sideband signal are presented at the output port (see column 2 and figure 1, 1021r-101r).

As per claim 28, Autechaud discloses the logic further operable to determine which of the decoders have identified real-data character types and those that have identified idle character types (see column 10).

As per claim 29, Autechaud discloses a system, further comprising alignment circuitry to align the real-data characters into a contiguous block with one of a left or right alignment relative to a delineated between the SOF and the EOF characters (see figure 1, column 2, 5-8, column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 30, Autechaud discloses a system, in which the controller is operable to store the aligned data characters in the storage registers when the total of the amount of aligned characters and the amount of characters in the storage register is less than or equal the width of the output port (see figure 1, column 2, 5-8, column 10, idle or null character is detected, real data SOF and EOF is checked).

As per claim 31, Autechaud discloses a system in which the controller is further operable to store a remaining portion of the aligned data characters in the storage register when the total exceeds the width of the output port (see figure 1, receive buffer and column 10).

As per claim 32, Autechaud et al. discloses a system, in which the controller is operable to output the stored characters of the storage registers responsive to the decoders and the logic determining an EOF character (see figure 1, block 101r).

As per claim 33, Turner discloses a system to interface a communication channel having a plurality of serial data lanes (abstract and figures 11 and 20), in which at least a portion of the receivers, the decoders, the logic, the parsing circuitry, the storage registers, and the controller comprise devices embedded within a programmable logic device; and another portion thereof comprise configured programmable resources of the programmable logic device (see abstract).

As per claim 34, Turner discloses a system to interface a communication channel having a plurality of serial data lanes (abstract and figures 11 and 20), in which the programmable logic device comprises configuration memory programmed with configuration data operable to configure the programmable resources adaptive to the number of serial data lanes of the communication channel (see figure 11 and 20).

As per claim 35, Turner et al. discloses a system to interface a communication channel having a plurality of serial data lanes (abstract and figures 11 and 20), in which the decoders comprise content addressable memories embedded within the programmable logic device and configurable per the programmable resources of the programmable logic device to receive characters of the receiver outputs and to source decode information to the logic (see abstract, figures 11 and 20).

As per claim 36, Autechaud et al. discloses a circuit to interface to a communications channel comprising: de-multiplexing means for recovering serial data from the data signals and converting the serial data into parallel data (see figure 1, decoder 108r, deserializer 109r, column 6-8); checking the parallel data for a start-of-frame (SOF) character (see figure 1, 1021r column 2, 6, 8); decode means for decoding characters recovered by the de- multiplexing means (see figure 1, decoder 108r, deserializer 109r, column 6-8); checking the parallel data for a start-of-frame (SOF) character (see figure 1, 1021r column 2, 6, 8); detection means for detecting at least one of a start-of- frame (SOF) character and an end-of-frame (EOF) character (see column 10, idle or null character is detected, real data SOF and EOF is checked); parser means for parsing characters based on type decoded and placement relative to a SOF character; and means for grouping together parsed characters (see column 2 and figure 1 1021r-101r).

Autechaud does not expressly disclose receiving a plurality of serial data signals from lanes of the communication channel.

Turner discloses receiving a plurality of serial data signals from lanes of the communication channel (see figure 11 and 20, column 2, 4).

Autechaud and Turner are analogous art since they are from the same field of endeavor of detecting and checking SOF and EOF in receivers.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to use Turner's lane assignment technique in Autechaud's device for checking and detecting SOF and EOF in receivers. The motivation being having a fair utilization of the method and apparatus of the high speed communication receiver by using a plurality of de-serializers, along with detecting and checking SOF and EOF in the receiver.

As per claim 37, Autechaud et al. discloses a circuit to interface to a communications channel, in which the decode means resolves character types of the group consisting of at least one of SOF, EOF, real data and idle data characters; and the parser means further bases the parsing upon whether the character placement is outside a frame delineated by at least one of a detected SOF character and a detected EOF character (see figure 1, decoder 108r, deserializer 109r, column 6-8).

As per claim 38, Autechaud et al. discloses a circuit to interface to a communications channel, in which the grouping means groups real data characters determined inside the frame with one of a left of right alignment (see figure 1, 1021r column 2, 6, 8).

As per claim 39, Autechaud et al. the parser means and the groupings means to group the data characters into a contiguous block having no idle characters (see figure 1, 1021r, column 2, 6, 8).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See form 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH RIYAMI whose telephone number is (571)270-3119. The examiner can normally be reached on Monday through Thursday 8am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Firmin Backer can be reached on (571)272-6703. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AR

2/27/08

BRIAN NGUYEN
PRIMARY EXAMINER